

## TFT LCD Approval Specification

### MODEL NO.: N133I1 - L02

Customer:

Approved by:

Note:

Liquid Crystal Display Division	
QRA Division.	OA Head Division.
Approval	Approval
	

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Issued Date: Apr. 7, 2006

Model No.: N133I1 - L02

**Approval****REVISION HISTORY**

Version	Date	Page (New)	Section	Description
2.0	Apr, 7, '06	All	All	Approval specification was first issued.



Issued Date: Apr. 7, 2006

Model No.: N133I1 - L02

Approval

## 1. GENERAL DESCRIPTION

### 1.1 OVERVIEW

N133I1 - L02 is a 13.3" TFT Liquid Crystal Display module with single CCFL Backlight unit and 20 pins LVDS interface. This module supports 1280 x 800 WXGA mode and can display 262,144 colors. The optimum viewing angle is at 6 o'clock direction. The inverter module for Backlight is not built in.

### 1.2 FEATURES

- Thin and Light Weight
- WXGA (1280 x 800 pixels) resolution
- DE only mode
- 3.3V LVDS (Low Voltage Differential Signaling) interface with 1 pixel/clock

### 1.3 APPLICATION

- TFT LCD Notebook

### 1.4 GENERAL SPECIFICATIONS

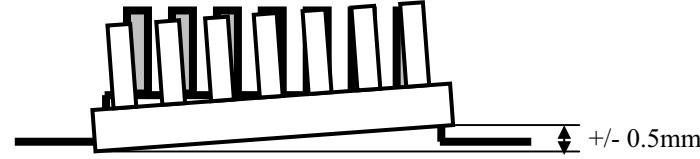
Item	Specification	Unit	Note
Active Area	286.08 (H) x 178.8 (V)	mm	(1)
Bezel Opening Area	289.1 (H) x 181.8 (V)	mm	
Driver Element	a-si TFT active matrix	-	-
Pixel Number	1280 x R.G.B. x 800	pixel	-
Pixel Pitch	0.2235 (H) x 0.2235 (V)	mm	-
Pixel Arrangement	RGB vertical stripe	-	-
Display Colors	262,144	color	-
Transmissive Mode	Normally white	-	-
Surface Treatment	Glare , 2H	-	-

### 1.5 MECHANICAL SPECIFICATIONS

Item	Min.	Typ.	Max.	Unit	Note
Module Size	Horizontal(H)	298.5	299	mm	(1)
	Vertical(V)	194.5	195	mm	
	Depth(D)	---	5.5	mm	
Weight	---	350	365	g	-
I/F connector mounting position	The mounting inclination of the connector makes the screen center within $\pm 0.5$ mm as the horizontal.		(2)		

Note (1) Please refer to the attached drawings for more information of front and back outline dimensions.

Note (2) Connector mounting position



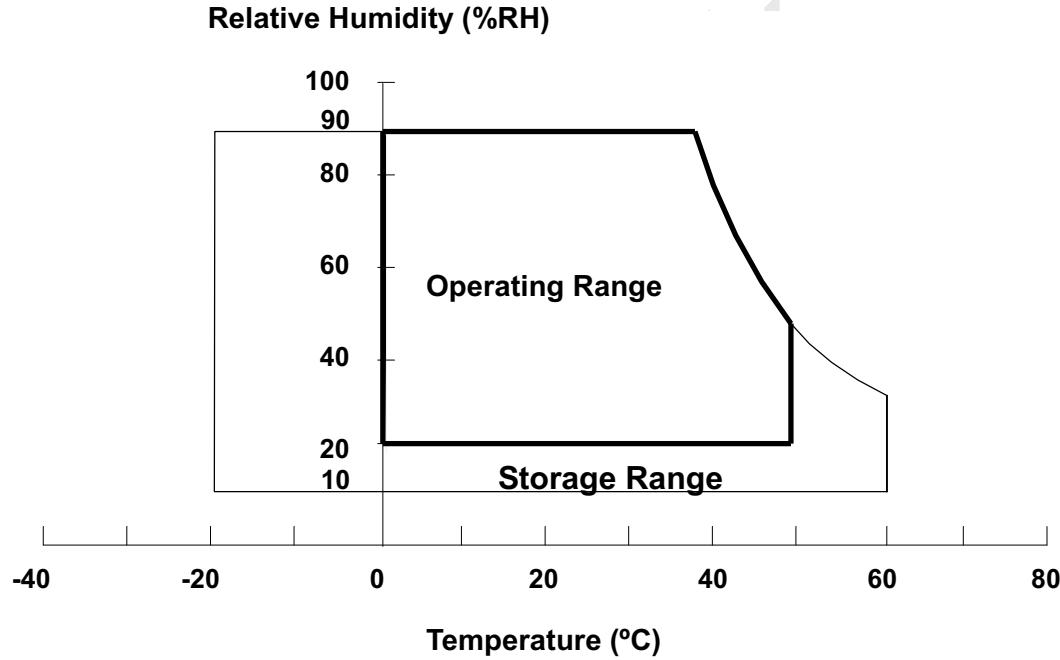
## 2. ABSOLUTE MAXIMUM RATINGS

### 2.1 ABSOLUTE RATINGS OF ENVIRONMENT

Item	Symbol	Value		Unit	Note
		Min.	Max.		
Storage Temperature	$T_{ST}$	-20	+60	°C	(1)
Storage Humidity	$H_{ST}$	10	90	%	
Operating Ambient Temperature	$T_{OP}$	0	+50	°C	(1), (2)
Operating Humidity	$H_{OP}$	20	90	%	
Shock (Non-Operating)	$S_{NOP}$	-	200/2	G/ms	(3), (5)
Vibration (Non-Operating)	$V_{NOP}$	-	1.5	G	(4), (5)

Note (1) Temperature and relative humidity range is shown in the figure below.

- (a) 90 %RH Max. ( $T_a \leq 40$  °C).
- (b) Wet-bulb temperature should be 39 °C Max. ( $T_a > 40$  °C).
- (c) No condensation.



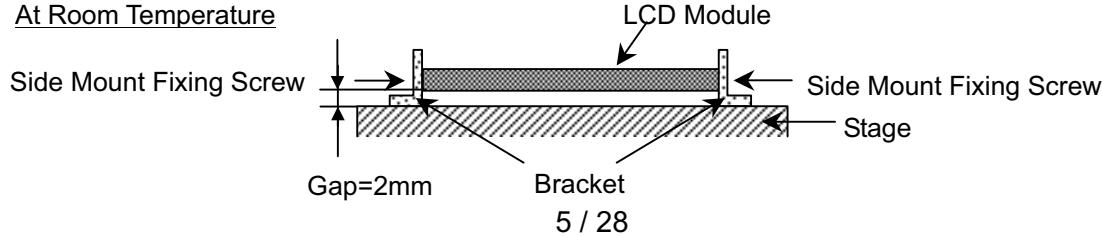
Note (2) The temperature of panel surface should be 0 °C Min. and 50 °C Max.

Note (3) 1 time for  $\pm X, \pm Y, \pm Z$ . for Condition (200G / 2ms) is half Sine Wave,

Note (4) 10 ~ 200 Hz, 0.5 Hr / Cycle, 1 cycles for each X, Y, Z.

Note (5) At testing Vibration and Shock, the fixture in holding the module has to be hard and rigid enough so that the module would not be twisted or bent by the fixture.

The fixing condition is shown as below:



The information described in this technical specification is tentative and it is possible to be changed without prior notice. Please contact CMO 's representative while your product design is based on this specification.

**Version 2.0**



## 2.2 ELECTRICAL ABSOLUTE RATINGS

### 2.2.1 TFT LCD MODULE

Item	Symbol	Value		Unit	Note
		Min.	Max.		
Power Supply Voltage	$V_{CC}$	-0.3	+4.0	V	
Logic Input Voltage	$V_{IN}$	-0.3	$V_{CC}+0.3$	V	(1)

### 2.2.2 BACKLIGHT UNIT

Item	Symbol	Value		Unit	Note
		Min.	Max.		
Lamp Voltage	$V_L$	--	2.5K	$V_{RMS}$	(1), (2), $I_L = 6.0$ mA
Lamp Current	$I_L$	2.0	7.0	$mA_{RMS}$	
Lamp Frequency	$F_L$	45	80	KHz	(1), (2)

Note (1) Permanent damage to the device may occur if maximum values are exceeded. Function operation should be restricted to the conditions described under Normal Operating Conditions.

Note (2) Specified values are for lamp (Refer to 3.2 for further information).

### 3. ELECTRICAL CHARACTERISTICS

#### 3.1 TFT LCD MODULE

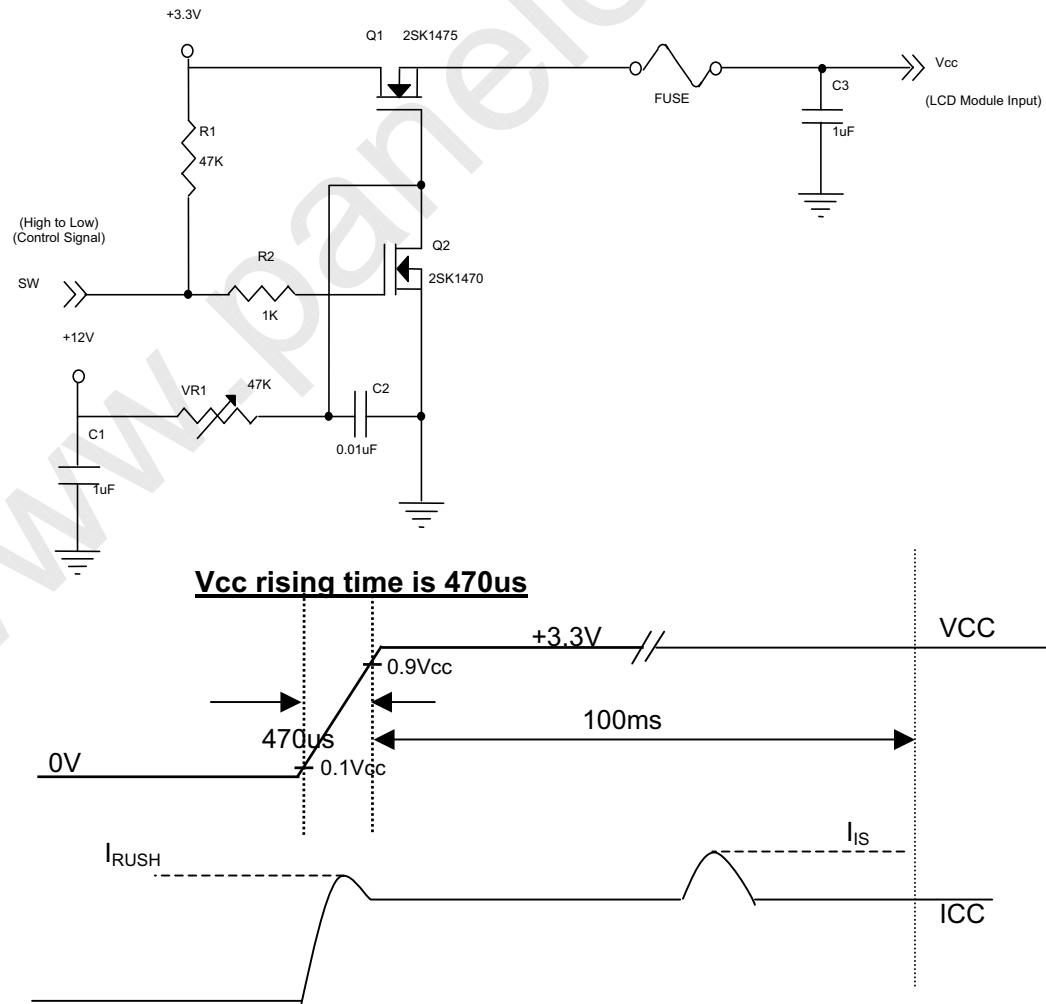
Parameter	Symbol	Value			Unit	Note
		Min.	Typ.	Max.		
Power Supply Voltage	V <sub>CC</sub>	3.0	3.3	3.6	V	-
Permissive Ripple Voltage	V <sub>RP</sub>		50		mV	-
Rush Current	I <sub>RUSH</sub>			1.5	A	(2)
Initial Stage Current	I <sub>IS</sub>			1.0	A	(2)
Power Supply Current	I <sub>CC</sub>		255	295	mA	(3)a
			330	375	mA	(3)b
LVDS Differential Input High Threshold	V <sub>TH(LVDS)</sub>			+100	mV	(5), V <sub>CM</sub> =1.2V
LVDS Differential Input Low Threshold	V <sub>TL(LVDS)</sub>	-100			mV	(5) V <sub>CM</sub> =1.2V
LVDS Common Mode Voltage	V <sub>CM</sub>	1.125		1.375	V	(5)
LVDS Differential Input Voltage	V <sub>ID</sub>	100		600	mV	(5)
Terminating Resistor	R <sub>T</sub>		100		Ohm	
Power per EBL WG	P <sub>EBL</sub>	-	2.62	-	W	(4)

Note (1) The ambient temperature is Ta = 25 ± 2 °C.

Note (2) I<sub>RUSH</sub>: the maximum current when VCC is rising

I<sub>IS</sub>: the maximum current of the first 100ms after power-on

Measurement Conditions: Shown as the following figure. Test pattern: black.



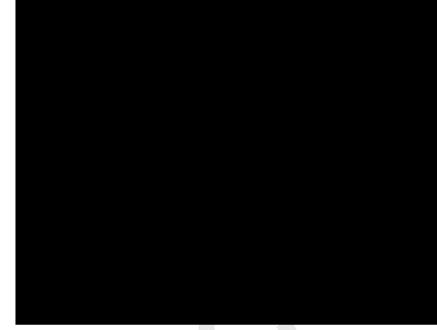
Note (3) The specified power supply current is under the conditions at  $V_{cc} = 3.3$  V,  $T_a = 25 \pm 2$  °C,  $f_v = 60$  Hz, whereas a power dissipation check pattern below is displayed.

a. White Pattern



Active Area

b. Black Pattern

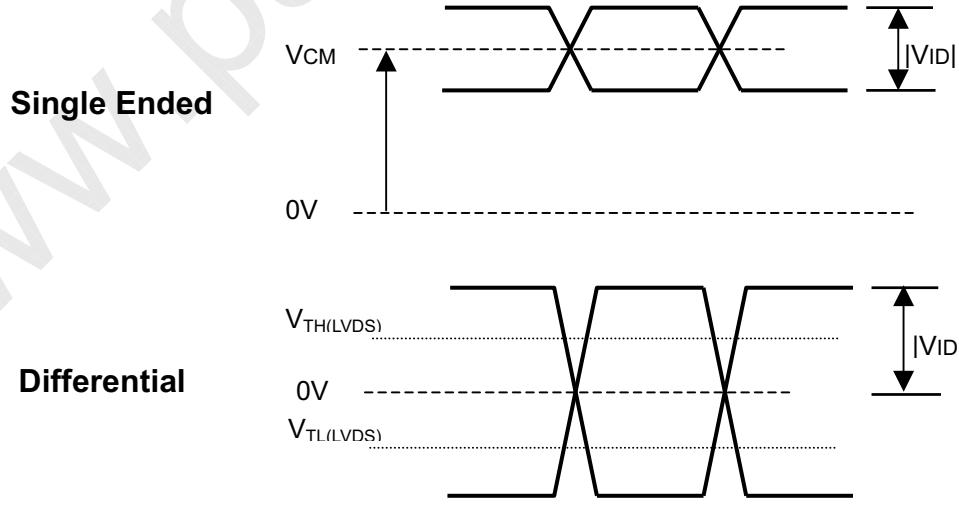


Active Area

Note (4) The specified power are the sum of LCD panel electronics input power and the inverter input power. Test conditions are as follows.

- (a)  $V_{cc} = 3.3$  V,  $T_a = 25 \pm 2$  °C,  $f_v = 60$  Hz,
- (b) The pattern used is a black and white 32 x 36 checkerboard, slide #100 from the VESA file "Flat Panel Display Monitor Setup Patterns", FPDMSU.ppt.
- (c) Luminance: 60 nits.
- (d) The inverter used is provided from Sumida ([www.sumida.com.tw](http://www.sumida.com.tw)). Please contact Sumida for detail information. CMO doesn't provide the inverter in this product.

Note (5) The parameters of LVDS signals are defined as the following figures.

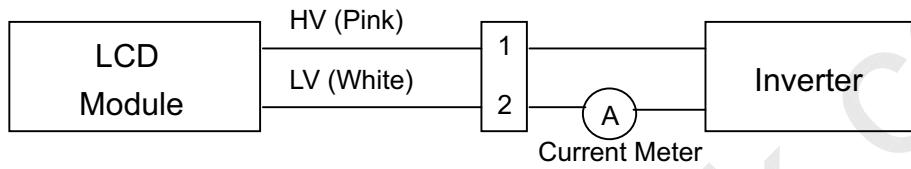


## 3.2 BACKLIGHT UNIT

 $T_a = 25 \pm 2 {}^\circ C$ 

Parameter	Symbol	Value			Unit	Note
		Min.	Typ.	Max.		
Lamp Input Voltage	$V_L$	576	640	704	$V_{RMS}$	$I_L = 6.0 \text{ mA}$
Lamp Current	$I_L$	2.0	6.0	7.0	$\text{mA}_{RMS}$	(1)
Lamp Turn On Voltage	$V_s$	---	---	1300 (25 °C)	$V_{RMS}$	(2)
		---	---	1450 (0 °C)	$V_{RMS}$	(2)
Operating Frequency	$F_L$	45	55	80	KHz	(3)
Lamp Life Time	$L_{BL}$	15,000	---	---	Hrs	(5)
Power Consumption	$P_L$	3.46	3.84	4.22	W	(4), $I_L = 6.0 \text{ mA}$

Note (1) Lamp current is measured by utilizing a high frequency current meter as shown below:



Note (2) The voltage that must be larger than  $V_s$  should be applied to the lamp for more than 1 second after startup. Otherwise, the lamp may not be turned on normally.

Note (3) The lamp frequency may produce interference with horizontal synchronous frequency from the display, and this may cause line flow on the display. In order to avoid interference, the lamp frequency should be detached from the horizontal synchronous frequency and its harmonics as far as possible.

Note (4)  $P_L = I_L \times V_L$

Note (5) The lifetime of lamp can be defined as the time in which it continues to operate under the condition  $T_a = 25 \pm 2 {}^\circ C$  and  $I_L = 6 \text{ mA}_{RMS}$  until one of the following events occurs:

- (a) When the brightness becomes or lower than 50% of its original value.
- (b) When the effective ignition length becomes or lower than 80% of its original value. (Effective ignition length is defined as an area that has less than 70% brightness compared to the brightness in the center point.)

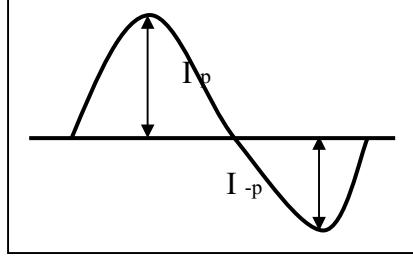
Note (6) The waveform of the voltage output of inverter must be area-symmetric and the design of the inverter must have specifications for the modularized lamp. The performance of the Backlight, such as lifetime or brightness, is greatly influenced by the characteristics of the DC-AC inverter for the lamp. All the parameters of an inverter should be carefully designed to avoid producing too much current leakage from high voltage output of the inverter. When designing or ordering the inverter please make sure that a poor lighting caused by the mismatch of the Backlight and the inverter (miss-lighting, flicker, etc.) never occurs. If the above situation is confirmed, the module should be operated in the same manners when it is installed in your instrument.

The output of the inverter must have symmetrical (negative and positive) voltage waveform and

symmetrical current waveform.(Unsymmetrical ratio is less than 10%) Please do not use the inverter which has unsymmetrical voltage and unsymmetrical current and spike wave. Lamp frequency may produce interface with horizontal synchronous frequency and as a result this may cause beat on the display. Therefore lamp frequency shall be as away possible from the horizontal synchronous frequency and from its harmonics in order to prevent interference.

Requirements for a system inverter design, which is intended to have a better display performance, a better power efficiency and a more reliable lamp. It shall help increase the lamp lifetime and reduce its leakage current.

- The asymmetry rate of the inverter waveform should be 10% below.
- The distortion rate of the waveform should be within  $\sqrt{2} \pm 10\%$ .
- The ideal sine wave form shall be symmetric in positive and negative polarities.



\* Asymmetry rate:

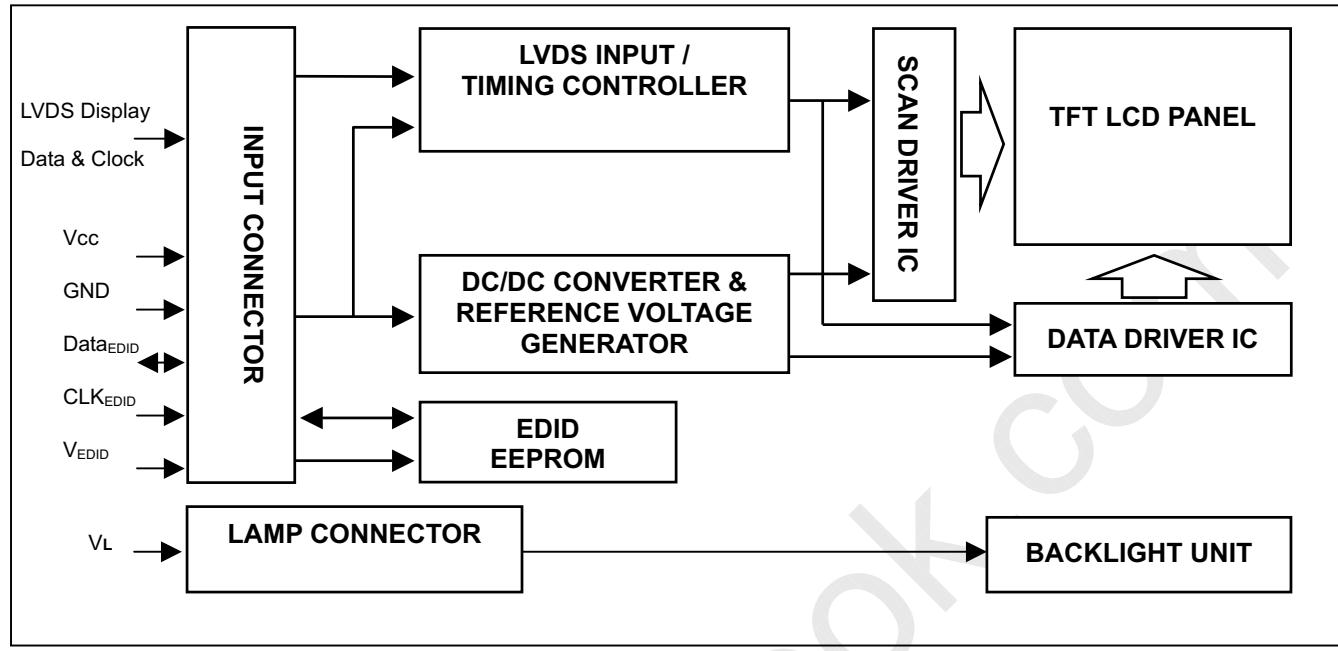
$$| I_p - I_{-p} | / I_{rms} * 100\%$$

\* Distortion rate

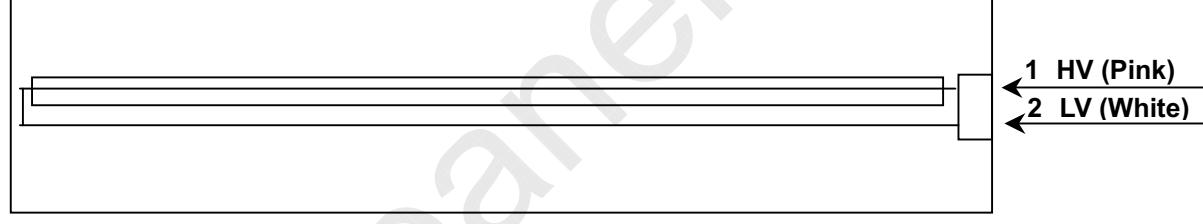
$$I_p \text{ (or } I_{-p}) / I_{rms}$$

## 4. BLOCK DIAGRAM

### 4.1 TFT LCD MODULE



### 4.2 BACKLIGHT UNIT



## 5. INPUT TERMINAL PIN ASSIGNMENT

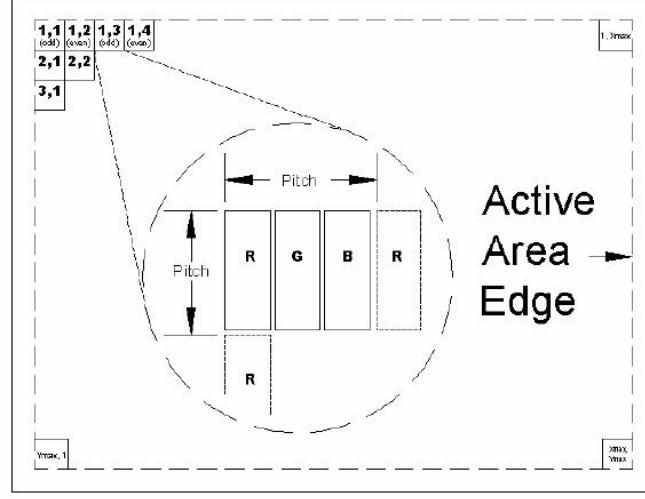
### 5.1 TFT LCD MODULE

Pin	Symbol	Description	Polarity	Remark
1	Vss	Ground		
2	Vcc	Power Supply +3.3 V (typical)		
3	Vcc	Power Supply +3.3 V (typical)		
4	V <sub>EDID</sub>	DDC 3.3V Power		DDC 3.3V Power
5	BIST	Panel BIST enable		
6	CLK <sub>EDID</sub>	DDC Clock		DDC Clock
7	DATA <sub>EDID</sub>	DDC Data		DDC Data
8	Rxin0-	LVDS Differential Data Input	Negative	R0~R5, G0
9	Rxin0+	LVDS Differential Data Input	Positive	
10	Vss	Ground		
11	Rxin1-	LVDS Differential Data Input	Negative	G1~G5, B0, B1
12	Rxin1+	LVDS Differential Data Input	Positive	
13	Vss	Ground		
14	Rxin2-	LVDS Differential Data Input	Negative	B2~B5, DE, Hsync, Vsync
15	Rxin2+	LVDS Differential Data Input	Positive	
16	Vss	Ground		
17	CLK-	LVDS Clock Data Input	Negative	LVDS Level Clock
18	CLK+	LVDS Clock Data Input	Positive	
19	Vss	Ground		
20	Vss	Ground		

Note (1) Connector Part No.: DF19KR-20P-1H (HIROSE) or equivalent

Note (2) User's connector Part No: DF-19G-20S-1SD or equivalent

Note (3) The first pixel is odd as shown in the following figure.



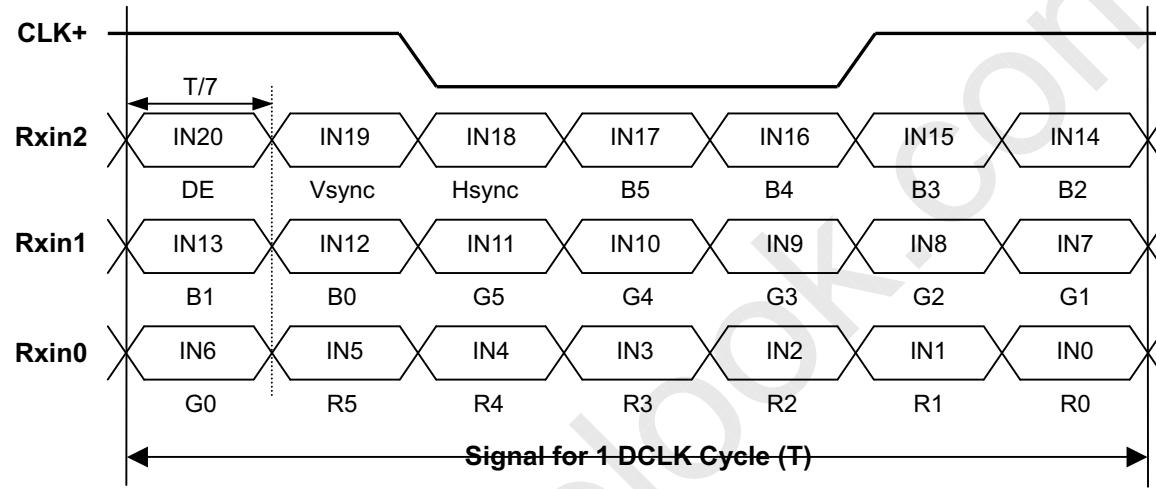
## 5.2 BACKLIGHT UNIT

Pin	Symbol	Description	Color
1	HV	High Voltage	Pink
2	LV	Ground	White

Note (1) Connector Part No.: JST- BHSR-02VS-1 or equivalent

Note (2) User's connector Part No.: SM02B-BHSS-1-TB or equivalent

## 5.3 TIMING DIAGRAM OF LVDS INPUT SIGNAL



## 5.4 COLOR DATA INPUT ASSIGNMENT

The brightness of each primary color (red, green and blue) is based on the 6-bit gray scale data input for the color. The higher the binary input, the brighter the color. The table below provides the assignment of color versus data input.

Color		Data Signal																			
		Red						Green						Blue							
		R5	R4	R3	R2	R1	R0	G5	G4	G3	G2	G1	G0	B5	B4	B3	B2	B1	B0		
Basic Colors	Black	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0
	Red	1	1	1	1	1	1	0	0	0	0	0	0	0	0	0	0	0	0	0	0
	Green	0	0	0	0	0	0	1	1	1	1	1	1	0	0	0	0	0	0	0	0
	Blue	0	0	0	0	0	0	0	0	0	0	0	0	1	1	1	1	1	1	1	1
	Cyan	0	0	0	0	0	0	1	1	1	1	1	1	1	1	1	1	1	1	1	1
	Magenta	1	1	1	1	1	1	0	0	0	0	0	0	1	1	1	1	1	1	1	1
	Yellow	1	1	1	1	1	1	1	1	1	1	1	1	0	0	0	0	0	0	0	0
	White	1	1	1	1	1	1	1	1	1	1	1	1	1	1	1	1	1	1	1	1
Gray Scale Of Red	Red(0)/Dark	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0
	Red(1)	0	0	0	0	0	1	0	0	0	0	0	0	0	0	0	0	0	0	0	0
	Red(2)	0	0	0	0	1	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0
	:	:	:	:	:	:	:	:	:	:	:	:	:	:	:	:	:	:	:	:	:
	Red(61)	1	1	1	1	0	1	0	0	0	0	0	0	0	0	0	0	0	0	0	0
	Red(62)	1	1	1	1	1	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0
	Red(63)	1	1	1	1	1	1	0	0	0	0	0	0	0	0	0	0	0	0	0	0
Gray Scale Of Green	Green(0)/Dark	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0
	Green(1)	0	0	0	0	0	0	0	0	0	0	0	0	0	1	0	0	0	0	0	0
	Green(2)	0	0	0	0	0	0	0	0	0	0	0	0	1	0	0	0	0	0	0	0
	:	:	:	:	:	:	:	:	:	:	:	:	:	:	:	:	:	:	:	:	:
	Green(61)	0	0	0	0	0	0	1	1	1	1	1	0	1	0	0	0	0	0	0	0
	Green(62)	0	0	0	0	0	0	1	1	1	1	1	0	1	0	0	0	0	0	0	0
	Green(63)	0	0	0	0	0	0	1	1	1	1	1	0	1	0	0	0	0	0	0	0
Gray Scale Of Blue	Blue(0)/Dark	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0
	Blue(1)	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0
	Blue(2)	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	1
	:	:	:	:	:	:	:	:	:	:	:	:	:	:	:	:	:	:	:	:	:
	Blue(61)	0	0	0	0	0	0	0	0	0	0	0	0	0	1	1	1	1	1	1	0
	Blue(62)	0	0	0	0	0	0	0	0	0	0	0	0	0	1	1	1	1	1	1	0
	Blue(63)	0	0	0	0	0	0	0	0	0	0	0	0	0	1	1	1	1	1	1	1

Note (1) 0: Low Level Voltage, 1: High Level Voltage

## 5.5 EDID DATA STRUCTURE

The EDID (Extended Display Identification Data) data formats are to support displays as defined in the VESA Plug & Display and FPDI standards.

Byte # (decimal)	Byte #(hex)	Field Name and Comments	Value (hex)	Value (binary)
0	0	Header	00	00000000
1	1	Header	FF	11111111
2	2	Header	FF	11111111
3	3	Header	FF	11111111
4	4	Header	FF	11111111
5	5	Header	FF	11111111
6	6	Header	FF	11111111
7	7	Header	00	00000000
8	8	EISA ID manufacturer name ("CMO")	0D	00001101
9	9	EISA ID manufacturer name (Compressed ASCII)	AF	10101111
10	0A	ID product code (N133I1-L02)	02	00000010
11	0B	ID product code (hex LSB first; N133I1-L02)	13	00010011
12	0C	ID S/N (fixed "0")	00	00000000
13	0D	ID S/N (fixed "0")	00	00000000
14	0E	ID S/N (fixed "0")	00	00000000
15	0F	ID S/N (fixed "0")	00	00000000
16	10	Week of manufacture (fixed week code)	09	00001001
17	11	Year of manufacture (fixed year code)	10	00010000
18	12	EDID structure version # ("1")	01	00000001
19	13	EDID revision # ("3")	03	00000011
20	14	Video I/P definition ("digital")	80	10000000
21	15	Active area horizontal 28.608cm	1D	00011101
22	16	Active area vertical 17.88cm	12	00010010
23	17	Display Gamma (Gamma = "2.2")	78	01111000
24	18	Feature support ("Active off, RGB Color")	0A	00001010
25	19	Red/Green (Rx1, Rx0, Ry1, Ry0, Gx1, Gx0, Gy1, Gy0)	65	01100101
26	1A	Blue/White (Bx1, Bx0, By1, By0, Wx1, Wx0, Wy1, Wy0)	21	00100001
27	1B	Red-x (Rx = "0.622")	9F	10011111
28	1C	Red-y (Ry = "0.346")	58	01011000
29	1D	Green-x (Gx = "0.333")	55	01010101
30	1E	Green-y (Gy = "0.528")	87	10000111
31	1F	Blue-x (Bx = "0.164")	2A	00101010
32	20	Blue-y (By = "0.162")	29	00101001
33	21	White-x (Wx = "0.313")	50	01010000
34	22	White-y (Wy = "0.329")	54	01010100
35	23	Established timings 1	00	00000000
36	24	Established timings 2	00	00000000
37	25	Manufacturer's reserved timings	00	00000000
38	26	Standard timing ID # 1	01	00000001
39	27	Standard timing ID # 1	01	00000001
40	28	Standard timing ID # 2	01	00000001
41	29	Standard timing ID # 2	01	00000001

42	2A	Standard timing ID # 3	01	00000001
43	2B	Standard timing ID # 3	01	00000001
44	2C	Standard timing ID # 4	01	00000001
45	2D	Standard timing ID # 4	01	00000001
46	2E	Standard timing ID # 5	01	00000001
47	2F	Standard timing ID # 5	01	00000001
48	30	Standard timing ID # 6	01	00000001
49	31	Standard timing ID # 6	01	00000001
50	32	Standard timing ID # 7	01	00000001
51	33	Standard timing ID # 7	01	00000001
52	34	Standard timing ID # 8	01	00000001
53	35	Standard timing ID # 8	01	00000001
54	36	Detailed timing description # 1 Pixel clock ("71MHz", According to VESA CVT Rev1.1)	BC	10111100
55	37	# 1 Pixel clock (hex LSB first)	1B	00011011
56	38	# 1 H active ("1280")	00	00000000
57	39	# 1 H blank ("160")	A0	10100000
58	3A	# 1 H active : H blank ("1280 : 160")	50	01010000
59	3B	# 1 V active ("800")	20	00100000
60	3C	# 1 V blank ("23")	17	00010111
61	3D	# 1 V active : V blank ("800 :23")	30	00110000
62	3E	# 1 H sync offset ("48")	30	00110000
63	3F	# 1 H sync pulse width ("32")	20	00100000
64	40	# 1 V sync offset : V sync pulse width ("3 : 6")	36	00110110
65	41	# 1 H sync offset : H sync pulse width : V sync offset : V sync width ("48: 32 : 3 : 6")	00	00000000
66	42	# 1 H image size ("286 mm")	1E	00011110
67	43	# 1 V image size ("179 mm")	B3	10110011
68	44	# 1 H image size : V image size ("286 : 179")	10	00010000
69	45	# 1 H boarder ("0")	00	00000000
70	46	# 1 V boarder ("0")	00	00000000
71	47	# 1 Non-interlaced, Normal, no stereo, Separate sync, H/V pol Negatives	18	00011000
72	48	Detailed timing description # 2	00	00000000
73	49	# 2 Flag	00	00000000
74	4A	# 2 Reserved	00	00000000
75	4B	# 2 FE (hex) defines ASCII string (Model Name "N133I1-L02", ASCII)	FE	11111110
76	4C	# 2 Flag	00	00000000
77	4D	# 2 1st character of name ("N")	4E	01001110
78	4E	# 2 2nd character of name ("I")	31	00110001
79	4F	# 2 3rd character of name ("L")	33	00110011
80	50	# 2 4th character of name ("O")	33	00110011
81	51	# 2 5th character of name ("P")	49	01001001
82	52	# 2 6th character of name ("E")	31	00110001
83	53	# 2 7th character of name ("R")	2D	00101101
84	54	# 2 8th character of name ("S")	4C	01001100
85	55	# 2 9th character of name ("T")	30	00110000
86	56	# 2 9th character of name ("2")	32	00110010



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87	57	# 2 New line character indicates end of ASCII string	0A	00001010
88	58	# 2 Padding with "Blank" character	20	00100000
89	59	# 2 Padding with "Blank" character	20	00100000
90	5A	Detailed timing description # 3	00	00000000
91	5B	# 3 Flag	00	00000000
92	5C	# 3 Reserved	00	00000000
93	5D	# 3 FE (hex) defines ASCII string (Vendor "CMO", ASCII)	FE	11111110
94	5E	# 3 Flag	00	00000000
95	5F	# 3 1st character of string ("C")	43	01000011
96	60	# 3 2nd character of string ("M")	4D	01001101
97	61	# 3 3rd character of string ("O")	4F	01001111
98	62	# 3 New line character indicates end of ASCII string	0A	00001010
99	63	# 3 Padding with "Blank" character	20	00100000
100	64	# 3 Padding with "Blank" character	20	00100000
101	65	# 3 Padding with "Blank" character	20	00100000
102	66	# 3 Padding with "Blank" character	20	00100000
103	67	# 3 Padding with "Blank" character	20	00100000
104	68	# 3 Padding with "Blank" character	20	00100000
105	69	# 3 Padding with "Blank" character	20	00100000
106	6A	# 3 Padding with "Blank" character	20	00100000
107	6B	# 3 Padding with "Blank" character	20	00100000
108	6C	Detailed timing description # 4	00	00000000
109	6D	# 4 Flag	00	00000000
110	6E	# 4 Reserved	00	00000000
111	6F	# 4 FE (hex) defines ASCII string (Model Name "N133I1-L02", ASCII)	FE	11111110
112	70	# 4 Flag	00	00000000
113	71	# 4 1st character of name ("N")	4E	01001110
114	72	# 4 2nd character of name ("1")	31	00110001
115	73	# 4 3rd character of name ("3")	33	00110011
116	74	# 4 4th character of name ("3")	33	00110011
117	75	# 4 5th character of name ("I")	49	01001001
118	76	# 4 6th character of name ("1")	31	00110001
119	77	# 4 7th character of name (" - ")	2D	00101101
120	78	# 4 8th character of name ("L")	4C	01001100
121	79	# 4 9th character of name ("0")	30	00110000
122	7A	# 4 9th character of name ("2")	32	00110010
123	7B	# 4 New line character indicates end of ASCII string	0A	00001010
124	7C	# 4 Padding with "Blank" character	20	00100000
125	7D	# 4 Padding with "Blank" character	20	00100000
126	7E	Extension flag	00	00000000
127	7F	Checksum	CF	11001111

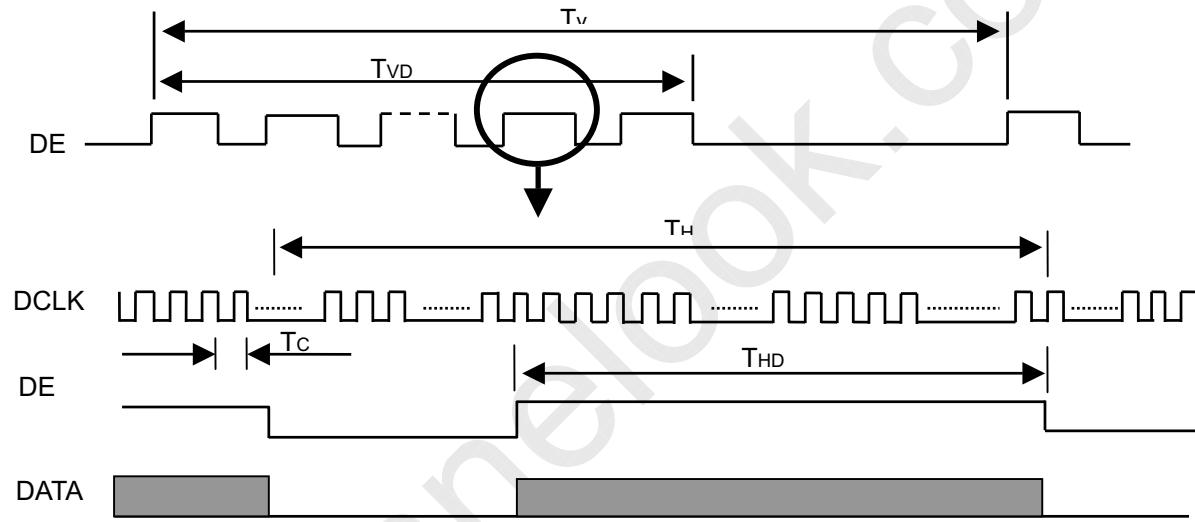
## 6. INTERFACE TIMING

### 6.1 INPUT SIGNAL TIMING SPECIFICATIONS

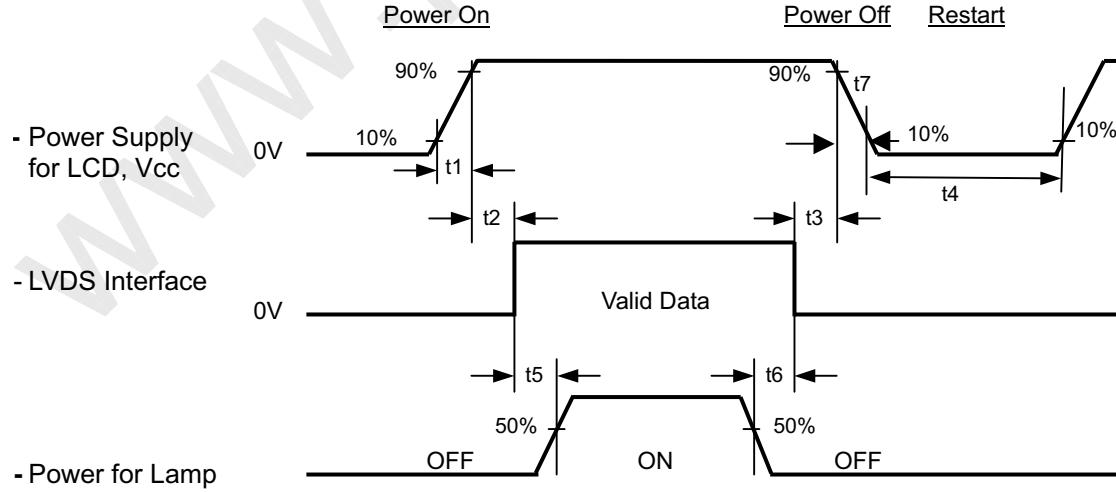
The specifications of input signal timing are as the following table and timing diagram.

Signal	Item	Symbol	Min.	Typ.	Max.	Unit	Note
DCLK	Frequency	1/Tc	50	71.1	80	MHz	-
DE	Vertical Total Time	TV	810	823	1900	TH	-
	Vertical Addressing Time	TVD	800	800	800	TH	-
	Horizontal Total Time	TH	1360	1440	1900	Tc	-
	Horizontal Addressing Time	THD	1280	1280	1280	Tc	-

INPUT SIGNAL TIMING DIAGRAM



### 6.2 POWER ON/OFF SEQUENCE





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## Timing Specifications:

$$0.5 \leq t1 \leq 10 \text{ ms}$$

$$0 \leq t2 \leq 50 \text{ ms}$$

$$0 \leq t3 \leq 50 \text{ ms}$$

$$t4 \geq 500 \text{ ms}$$

$$t5 \geq 200 \text{ ms}$$

$$t6 \geq 200 \text{ ms}$$

Note (1) Please follow the power on/off sequence described above. Otherwise, the LCD module might be damaged.

Note (2) Please avoid floating state of interface signal at invalid period. When the interface signal is invalid, be sure to pull down the power supply of LCD Vcc to 0 V.

Note (3) The Backlight inverter power must be turned on after the power supply for the logic and the interface signal is valid. The Backlight inverter power must be turned off before the power supply for the logic and the interface signal is invalid.

Note (4) Sometimes some slight noise shows when LCD is turned off (even backlight is already off). To avoid this phenomenon, we suggest that the Vcc falling time is better to follow  $5 \leq t7 \leq 300 \text{ ms}$ .



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## 7. OPTICAL CHARACTERISTICS

### 7.1 TEST CONDITIONS

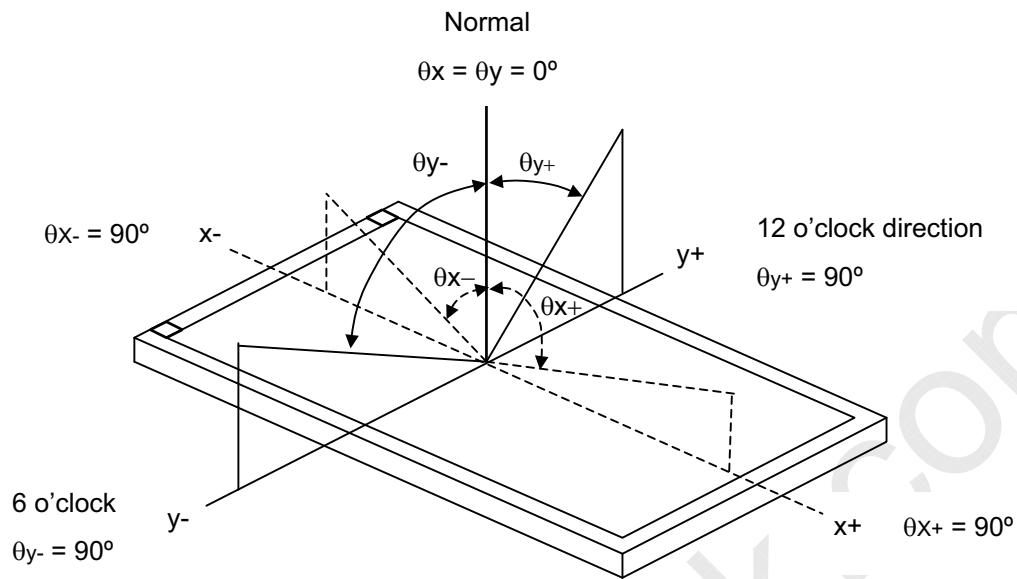
Item	Symbol	Value	Unit
Ambient Temperature	T <sub>a</sub>	25±2	°C
Ambient Humidity	H <sub>a</sub>	50±10	%RH
Supply Voltage	V <sub>CC</sub>	3.3	V
Input Signal	According to typical value in "3. ELECTRICAL CHARACTERISTICS"		
Inverter Current	I <sub>L</sub>	6	mA
Inverter Driving Frequency	F <sub>L</sub>	61	KHz
Inverter	Sumida-H05-4915		

The relative measurement methods of optical characteristics are shown in 7.2. The following items should be measured under the test conditions described in 7.1 and stable environment shown in Note (6).

### 7.2 OPTICAL SPECIFICATIONS

Item	Symbol	Condition	Min.	Typ.	Max.	Unit	Note
Contrast Ratio	CR	$\theta_x=0^\circ, \theta_y=0^\circ$ Viewing Normal Angle	350	500		-	(2), (5)
Response Time	T <sub>R</sub>		-	5	10	ms	(3)
	T <sub>F</sub>		-	11	16	ms	
Average Luminance of White	L <sub>AVE</sub>		210	250		cd/m <sup>2</sup>	(4), (5)
White Variation	$\delta W$				1.4	-	(5), (6)
Color Chromaticity	Red		0.602			-	(1)
	R <sub>x</sub>		0.340			-	
	R <sub>y</sub>		0.330			-	
	Green		0.543			-	
	G <sub>x</sub>		-0.03	0.158		+0.03	
	G <sub>y</sub>		0.146			-	
Viewing Angle	Blue	CR≥10	0.313			-	Deg.
	B <sub>x</sub>		0.329			-	
	B <sub>y</sub>		40	45			
	White		40	45			
	Horizontal		40	45			Deg.
	$\theta_x+$		15	20			
	$\theta_x-$		40	45			
	Vertical		40	45			
	$\theta_y+$						Deg.
	$\theta_y-$						

Note (1) Definition of Viewing Angle ( $\theta_x, \theta_y$ ):



Note (2) Definition of Contrast Ratio (CR):

The contrast ratio can be calculated by the following expression.

$$\text{Contrast Ratio (CR)} = L_{63} / L_0$$

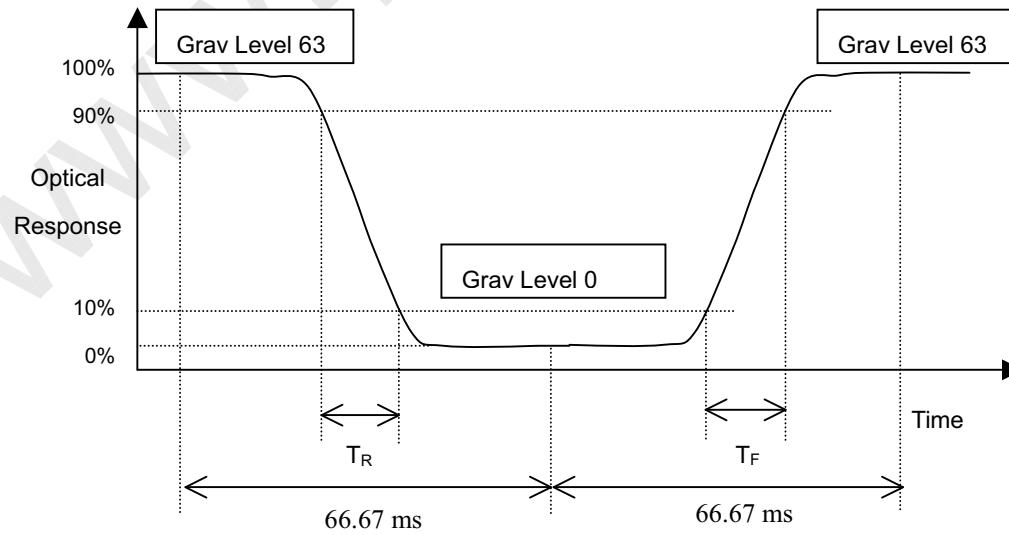
$L_{63}$ : Luminance of gray level 63

$L_0$ : Luminance of gray level 0

$$CR = CR (5)$$

CR (X) is corresponding to the Contrast Ratio of the point X at Figure in Note (7).

Note (3) Definition of Response Time ( $T_R, T_F$ ) and measurement method:



Note (4) Definition of Average Luminance of White ( $L_{AVE}$ ):

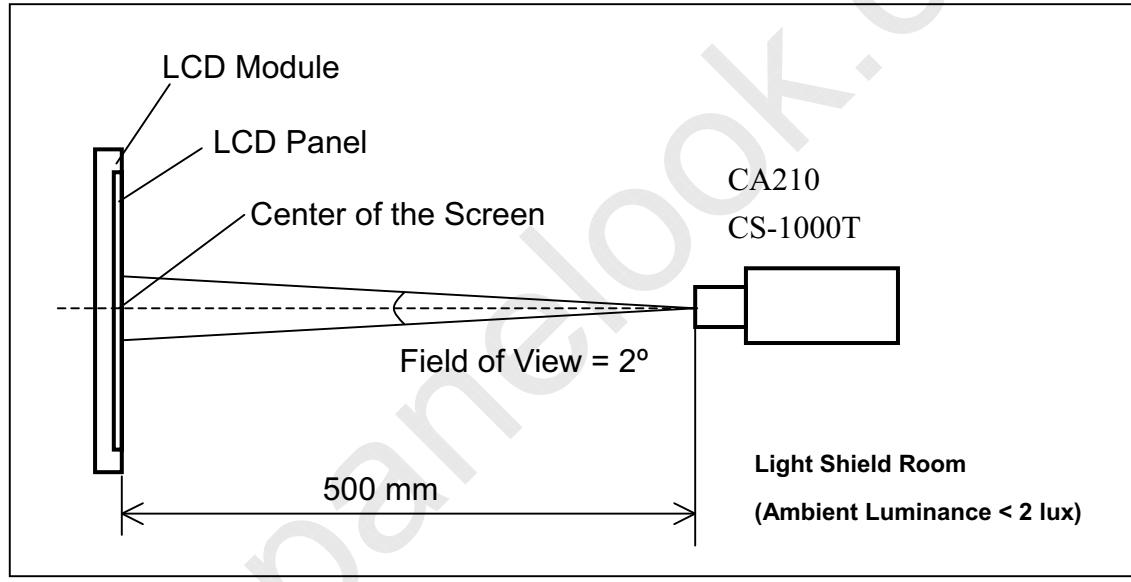
Measure the luminance of gray level 63 at 5 points

$$L_{AVE} = [L(1) + L(2) + L(3) + L(4) + L(5)] / 5$$

$L(x)$  is corresponding to the luminance of the point X at Figure in Note (6).

Note (5) Measurement Setup:

The LCD module should be stabilized at given temperature for 20 minutes to avoid abrupt temperature change during measuring. In order to stabilize the luminance, the measurement should be executed after lighting Backlight for 20 minutes in a windless room.

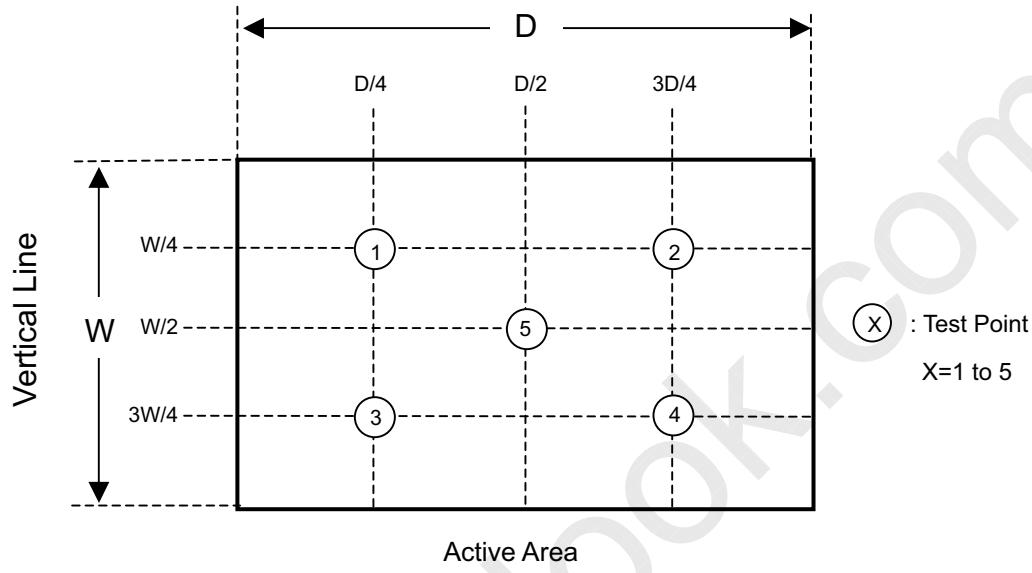


Note (6) Definition of White Variation ( $\delta W$ ):

Measure the luminance of gray level 63 at 5 points

$$\delta W = \text{Maximum} [L(1), L(2), L(3), L(4), L(5)] / \text{Minimum} [L(1), L(2), L(3), L(4), L(5)]$$

Horizontal Line





## 8. PRECAUTIONS

### 8.1 ASSEMBLY AND HANDLING PRECAUTIONS

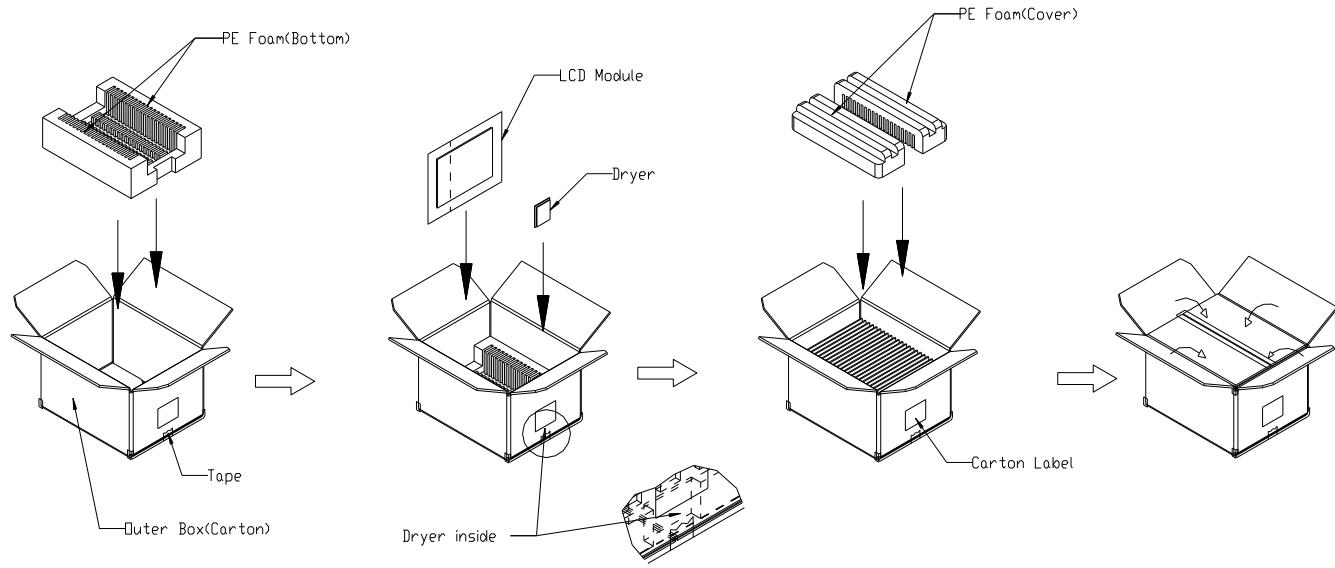
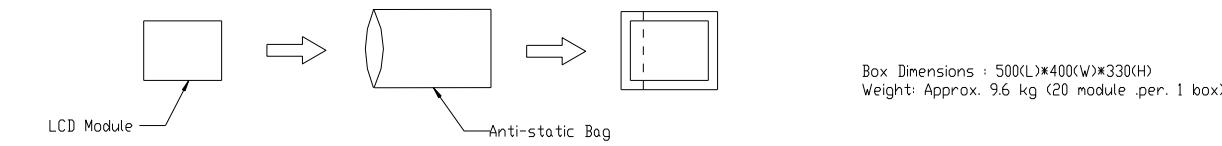
- (1) Do not apply rough force such as bending or twisting to the module during assembly.
- (2) To assemble or install module into user's system can be only in clean working areas. The dust and oil may cause electrical short or worsen the polarizer.
- (3) It's not permitted to have pressure or impulse on the module because the LCD panel and Backlight will be damaged.
- (4) Always follow the correct power sequence when LCD module is connecting and operating. This can prevent damage to the CMOS LSI chips during latch-up.
- (5) Do not pull the I/F connector in or out while the module is operating.
- (6) Do not disassemble the module.
- (7) Use a soft dry cloth without chemicals for cleaning, because the surface of polarizer is very soft and easily scratched.
- (8) It is dangerous that moisture come into or contacted the LCD module, because moisture may damage LCD module when it is operating.
- (9) High temperature or humidity may reduce the performance of module. Please store LCD module within the specified storage conditions.
- (10) When ambient temperature is lower than 10°C may reduce the display quality. For example, the response time will become slowly, and the starting voltage of CCFL will be higher than room temperature.

### 8.2 SAFETY PRECAUTIONS

- (1) The startup voltage of Backlight is approximately 1000 Volts. It may cause electrical shock while assembling with inverter. Do not disassemble the module or insert anything into the Backlight unit.
- (2) If the liquid crystal material leaks from the panel, it should be kept away from the eyes or mouth. In case of contact with hands, skin or clothes, it has to be washed away thoroughly with soap.
- (3) After the module's end of life, it is not harmful in case of normal operation and storage.

## 9. PACKAGING

### 9.1 CARTON



**Figure. 9-1 Packing method**

## 9.2 PALLET

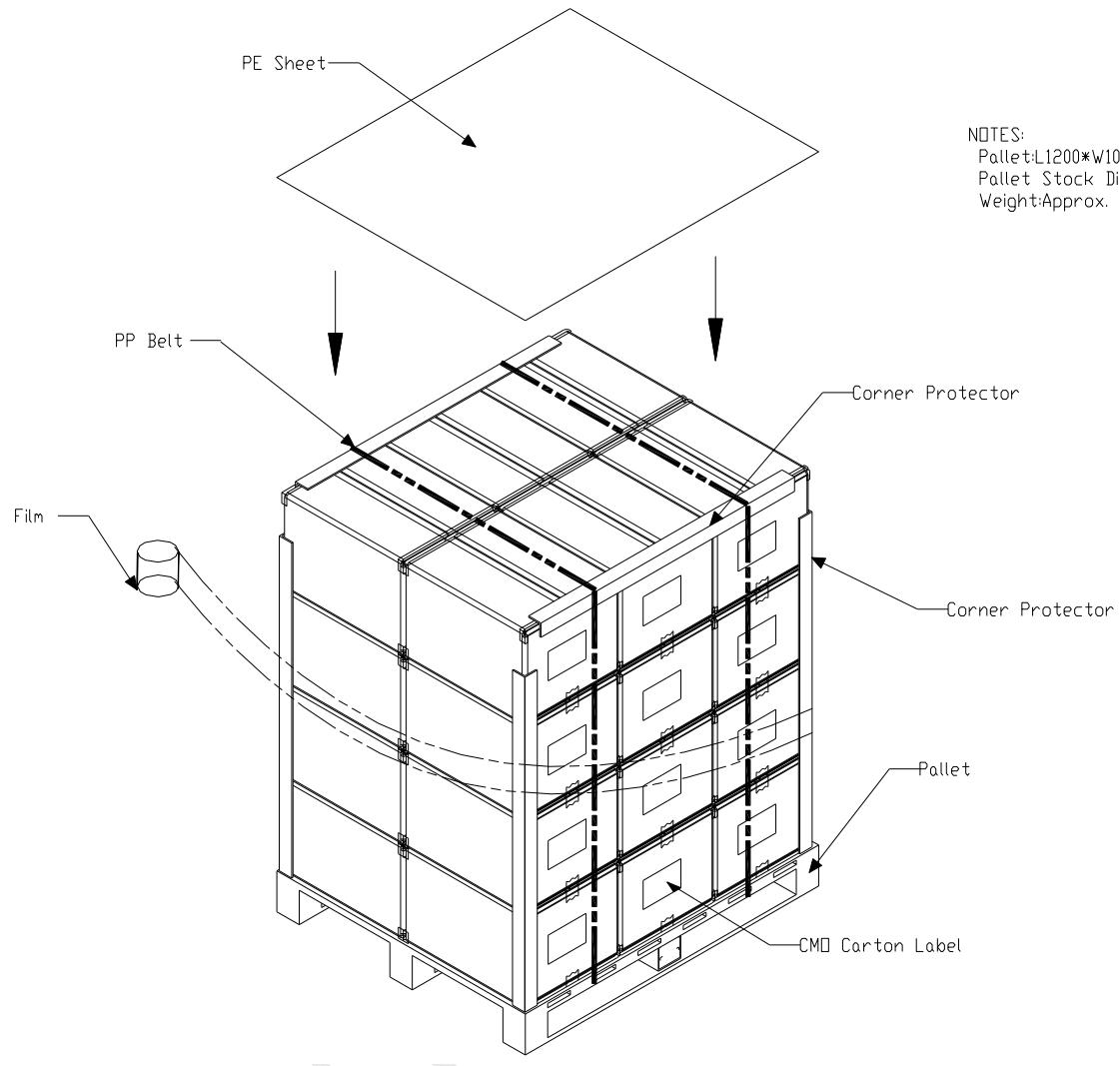


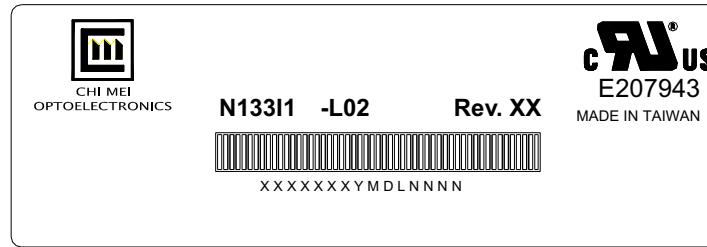
Figure. 9-2 Packing method



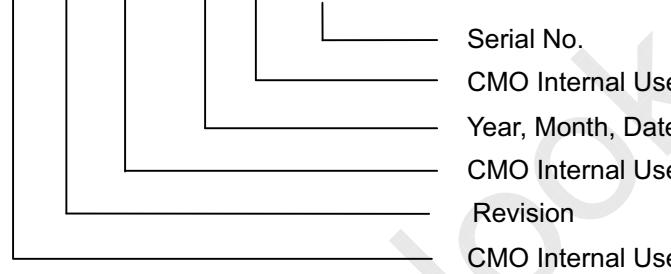
## 10. DEFINITION OF LABELS

### 10.1 CMO MODULE LABEL

The barcode nameplate is pasted on each module as illustration, and its definitions are as following explanation.



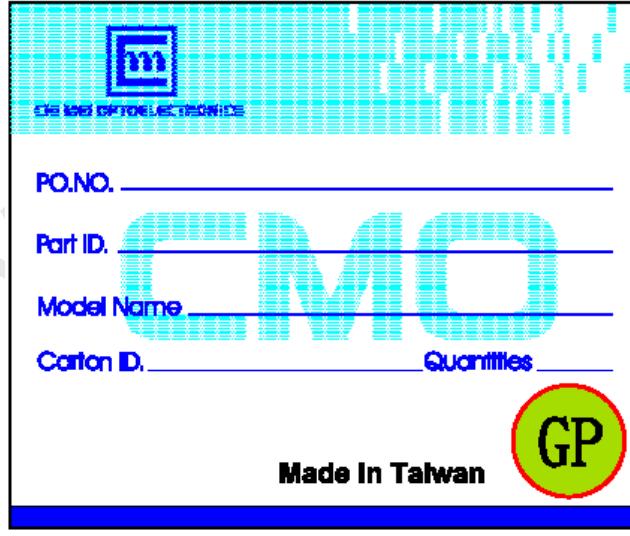
- (a) Model Name: N133I1 - L02
- (b) Revision: Rev. XX, for example: A1, ..., C1, C2 ...etc.
- (c) Serial ID: XX XX XX XX Y M D X N N N

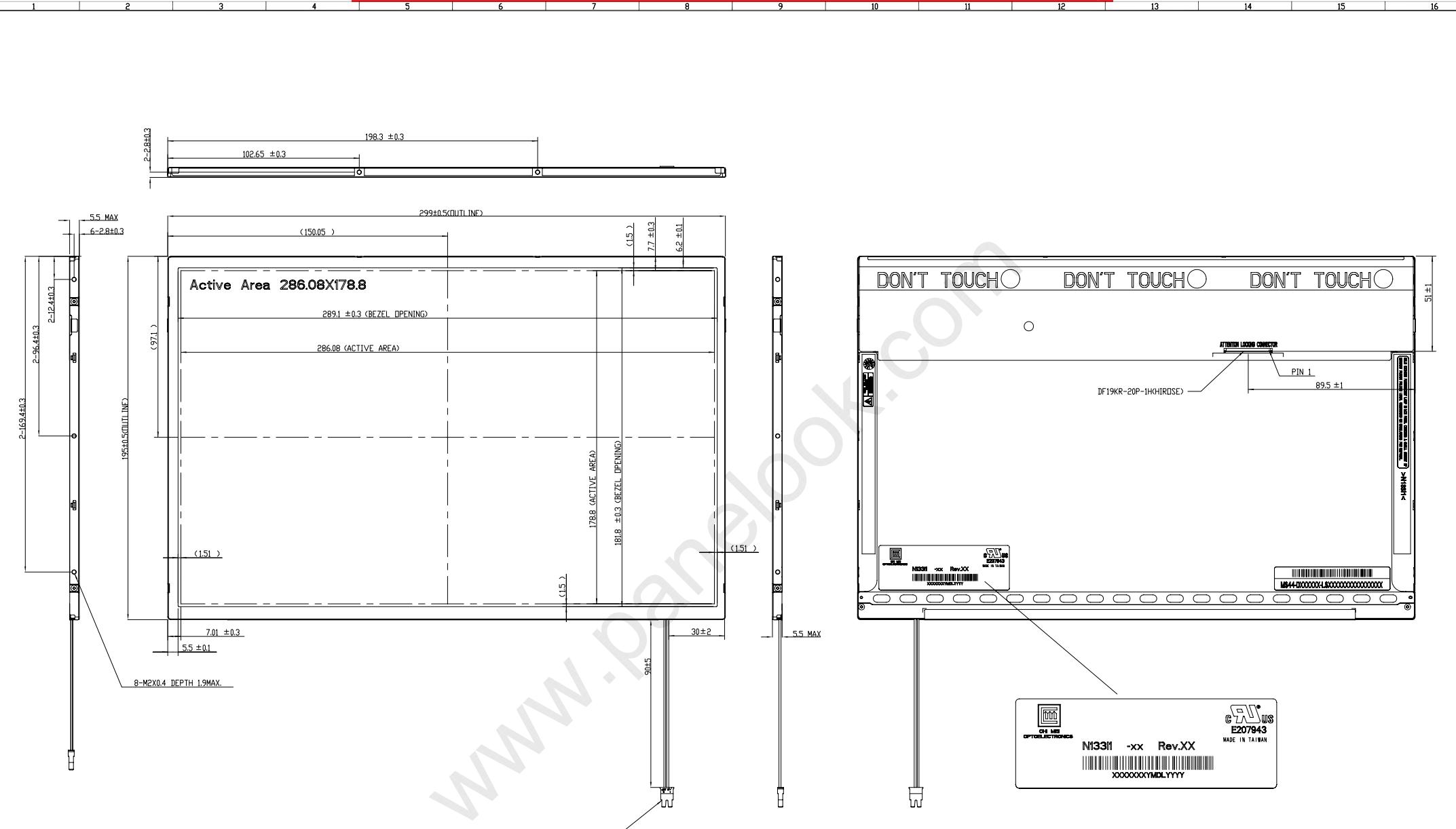


Serial ID includes the information as below:

- (a) Manufactured Date: Year: 1~9, for 2001~2009  
 Month: 1~9, A~C, for Jan. ~ Dec.  
 Day: 1~9, A~Y, for 1<sup>st</sup> to 31<sup>st</sup>, exclude I, O and U
- (b) Revision Code: cover all the change
- (c) Serial No.: Manufacturing sequence of product

### 10.2 CMO CARTON LABEL





NOTES:  
1. OUTLINE TOLERANCE:  $\pm 0.5\text{mm}$ .  
2. \* MARKS THE DESIGN CRITICAL DIMENSION.  
3.  $\oplus$  MARKS THE PROCESS CRITICAL DIMENSION  
4. MAX SCREW LENGTH: 1.9 mm.  
5. MAX SCREW TORQUE: 2.0 kg-cm.

H						
Mark	Description	Date	Changed_By	Approved_By	ECN No.	Remark

TITLE	ASSY_MODULE_N1331-L02			2D REV.0
				3D REV.0
Approved	BILL_SHEU	Drawing No.	N1331412II	
Checked	YUKE_LIN	Part No.	TBD	
Drawer	YADICHEN_CHEN	Material	TBD	Sheet 1 / 1 A
Designer	YADICHEN_CHEN	Date	25-Aug-2005	Scale 1:1 Unitmm
 CHI MEI OPTOELECTRONICS CORP. ALL RIGHTS RESERVED, COPYING FORBIDDEN.				